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DESIGN OF AN ENERGY EFFICIENT MULTIPLIER USING COMPLEMENTARY ENERGY PATH ADIABATIC LOGIC

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Abstract: The paper presents a new adiabatic multiplier circuit based on Complementary Energy Path Adiabatic Logic (CEPAL). The proposed multiplier consumes lesser power when compared to the conventional CMOS multiplier. The proposed adiabatic array multiplier performs 4 X 4 bit multiplication. The proposed adiabatic multiplier is also designed with leakage reduction technique the performance of which is better when compared to the CMOS multiplier. The operating speed of the complementary metal oxide semiconductor is increased. This paper presents the implementation of adiabatic CEPAL multiplier using CMOS. The measurement results of the adiabatic CMOS Multiplier demonstrate a reduction in power and reduction in energy. The operating frequency is in GHz range. These results show that the proposed circuit can be used in high speed application. The proposed adiabatic circuits are designed in HSPICE using predictive technology models (PTM) in 32nm CMOS Technology. The experimental results for the proposed adiabatic designs demonstrate their effectiveness with energy consumption and with power optimization.

1. INTRODUCTION

In recent times, mobile devices are emerging in faster rate replacing the existing devices which are bulky and consume more power. The mobile devices have high device density and are computationally faster. But increase in device density increases the power consumption. Circuits fabricated in CMOS technology below 65nm have less control over temperature and power wastage happens due to leakage current. Even though full swing voltage mode CMOS logic styles have been extremely successful they suffer from the lower limit of power dissipation on $C_L V_{dd}^2/2$ during switching instants. So new methodologies and technologies are evolved to solve the problems occurring due to undesired power dissipation. Adiabatic circuits have power dissipation lower than the limit level of CMOS. But the speed of operation reduces. The total energy is reduced through energy

recycling which is the basic concept behind adiabatic. Power supplies are pulse shaped and to be designed separately to meet the required load. In literature the adiabatic circuits are proved to have the best performance in power consumption. For computing units in processor core, faster and low power processing elements (PE) are required. Circuits like inverters, adders, multipliers, shifters and latch form the basic building blocks of a microprocessor or digital signal processor. Several adiabatic logics are proposed in literature like ECRL [1], differential logic [2], Dual rail[3], pass transistor [4] etc. In the literature chanda et al [5] proposed a multiplier architecture based on Urdhva Tiryakbhyam in CMOS adiabatic logic. A NxN vedic multiplier is designed using sum block, carry block and NAND-AND adiabatic block. For the implementation energy efficient adiabatic logic (EEAL) is used. The work is carried out in 180nm technology. The power can be further modified in this work by implementing in a 90nm technology or utilizing a different adiabatic logic instead of EEAL.

Cancio Monteiro et al [6] proposed a charge-sharing symmetric adiabatic logic (CSSAL) multiplier. The paper reports the NAND/NOR logic and their implementation in multiplier. The advantage of the presented circuit is that the internal nodes of the circuit are maintained at same charge for the different combinations of input. The disadvantage is the less successful of the method at higher frequencies so used in cryptography applications. In literature [7] a two phase clocked adiabatic static CMOS based Baugh wooley and Wallace tree multiplier is designed. The paper reports that the Wallace tree Multiplier shows less power consumption about 62.66% compared to Baugh wooley multiplier. The implementation is done in 45nm which is troublesome when leakage current is considered.

Hardik Sangani et al [8] proposed a multiplier based on the classical ancient Indian vedic sutras. The structure of the multiplier is based on energy recovery logic. The operating frequency reported was 25MHz at 45nm which is lower. Similar work is done in the literature [9], a vedic multiplier implementation using CMOS, PFAL and ECRL. The work presents that the PFAL circuit provides better performance when compared to CMOS and ECRL. Still other multipliers were designed using Adiabatic XOR gates and sleep mode transistor logic [10]. A combination of subthreshold circuit and adiabatic logic design is utilized for the design of a multiplier. The circuit is driven by two power supply which is an AC signals with different amplitude and frequencies. The

implementation is done in 180nm technology with skew tolerance circuit. A 4×4-bit Multiplier LSI Implementation of Two Phase Clocking Subthreshold Adiabatic Logic was done. An adiabatic ultra low power multiplier is proposed in literature [11]. The reported frequency of operation is 1 kHz.

1.1 ADIABATIC CEPAL STRUCTURE

The limitations in irreversible ERL adiabatic logics are high switching activity caused by the most dynamic characteristics, need for multiphase and multiple-clock operations, design of a trapezoid or triangular PC(s), interlaced circuit configuration, differential signaling and output floating. The other problems occurring are oscillations of PCs through output tracking which causes power loss during adiabatic switching. Even in the QSERL circuit the throughput is closely related to the frequency ratio of the input to PCs and a valid logic at the input must occupy a whole PC cycle including the evaluation and hold phases otherwise the circuit may fail during evaluation. These problems lead to noise susceptance due to floating in output.

The CEPAL structure is given in figure.1 , M4 and M3 are charging transistors and M1 and M2 are discharging transistors. With a pull-up and a pull-down network the structure has two paths. For the initial operation assuming that the output is LOW, the pull up network is ON while the pull down
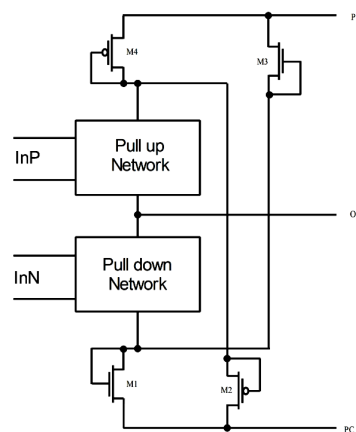

Fig. 1. Structure of a CEPAL logic

network is OFF, the output follows either PC or its complement as it swings HIGH. This makes the power clock swinging down and the output node to become floating. But this situation is immediately

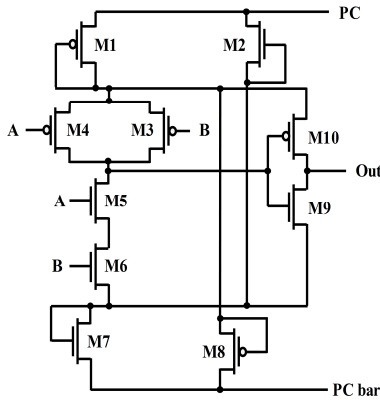removed when the power clock swings up. The CEPAL based AND gate is shown in figure 2.

Fig. 2. CEPAL AND gate structure.

1.2 Processing elements in DSP architectures

In DSP applications design of Filters is the critical block which deals with lot of computational units. The filter structure differs from application to algorithm specific. The adders, multipliers, shift registers, inverters, buffers are the different components of the filter structure. The multiplier is the most critical unit and requires an optimized structure based on partial product reduction, multioperand options etc. In multipliers the partial products are first generated and finally combined to obtain the final product. In this work the multiplier is optimized in the adder block where the number of transistors is reduced by 80% compared to the conventional adders. For partial product generators the array multiplier and Vedic multiplier are implemented using adiabatic logics. The adder designed in this work is based on CEPAL adiabatic logic. As explained earlier, the adder design is a prime concern for the implementation of an efficient multiplier. The proposed adder shown in figure 3 is more suitable for efficient implementation of large operand adders. However, these designs are very efficient in terms of power consumption but special power clock generator circuits are required which is not the scope of this paper.
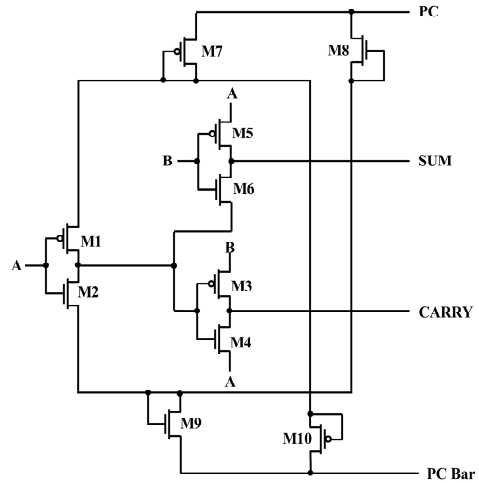

Fig. 3. CEPAL half Adder structure.

Multiplier

Array multipliers are easy to design and smaller in size. As the name indicates array multiplier uses parallelogram technique in its operation. All the partial products are generated at the same time. The combining adder receives the partial products as inputs and produces the output. The multiplier is suitable for performing matrix multiplication. The structure is regular such that the vertical and horizontal delays are same. The critical path delays in the terms of full adder and gate have same value. Implementation of DSP algorithms with pipelining can be made easy using array multipliers. Array multiplier is shown in figure 4.

1.3 PROPOSED CMOS CEPAL MULTIPLIER

CMOS based adiabatic CEPAL processing element implementation using half adder, full adder and multiplier is proposed. The proposed array multiplier block diagram is shown in figure 5. The implementation of the proposed circuit for multiplier is shown in figure 6. For the implementation predictive technology model for 32nm is used. The supply voltage is 1V. The number of transistors is 14, 10 and 76 for full adder, half adder and multiplier respectively. XOR and AND gate having 14 transistors and 6 transistors respectively are used for the design of adder. The array structure for 8 bit results is shown. The circuit is faster in the operation and consumes lesser power and energy. The power and energy analysis for the

conventional and proposed half adder is shown in table 1.

From table 2 the results show that the power dissipation in conventional FA is more compared to the proposed. The proposed multiplier dominates and outperforms the Vedic multiplier design. The Vedic multiplier is faster when implemented in a non adiabatic way but still suffers from the number of transistors used. But when comes to adiabatic logic, the CMOS CEPAL based multiplier performance is better. Table 3 shows the comparison table for the two multipliers. The circuit runs with a power clock of 1 GHz.

1.4 CONCLUSION

A new adiabatic multiplier circuit based on Complementary Energy Path Adiabatic Logic (CEPAL) is proposed in this paper. The proposed multiplier consumes less power and energy when compared to the conventional multiplier. The proposed adiabatic array multiplier performs 4 X 4 multiplication and is designed with leakage reduction technique. The measurement results of the half adder, full adder and adiabatic CMOS Multiplier demonstrates a reduction in power and reduction in energy. The power clock frequency is set to 1GHz. The implementations were carried out using HSPICE tool with predictive technology models (PTM) in 32nm CMOS Technology.

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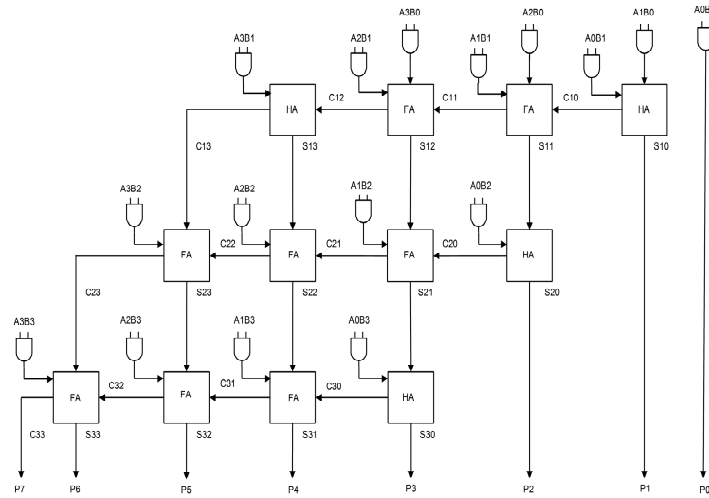
Fig. 4. Array multiplier using conventional adders.

Table 1. Power and energy analysis of Half adder

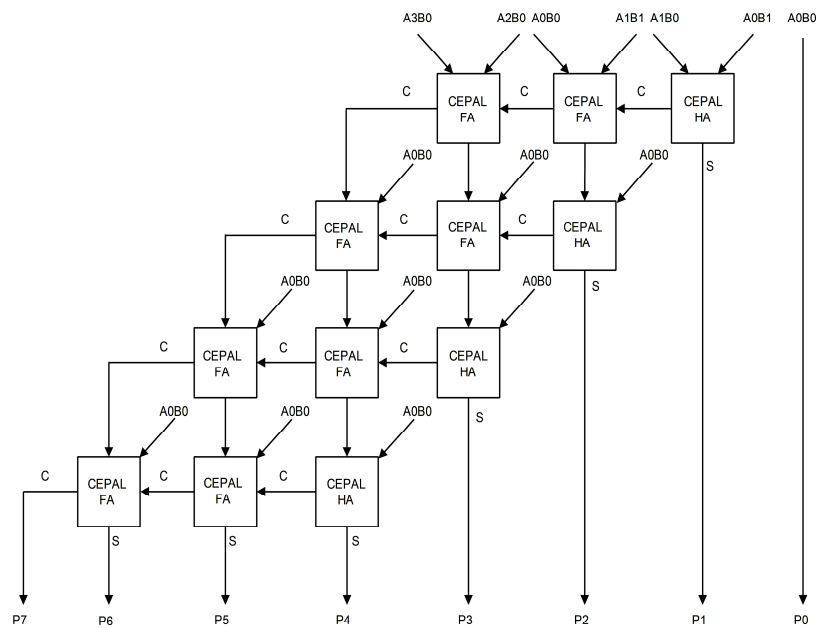| Circuit	CMOS		
	P_{avg} in µW	I_{avg} in µA	E in fJ
Conventional Half Adder	0.3976	0.3976	198.8
CEPAL Half Adder type 1	0.1134	0.0149	56.944
CEPAL Half Adder type 2	0.092	0.0138	46.268

Fig. 5. Proposed Array multiplier using CEPAL adiabatic logic.

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Table 2. Power and energy analysis of Full adder

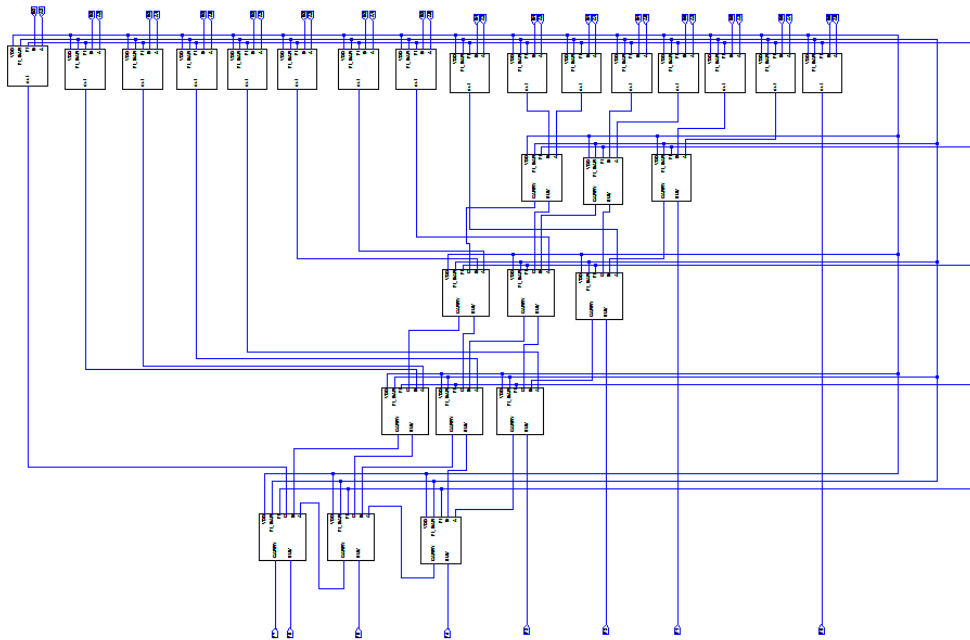| Circuit	CMOS		
	P_{avg} in µW	I_{avg} in µA	E in fJ
Conventional Full Adder	1.0844	1.0844	542.2
CEPAL Full Adder type 1	0.1159	0.0621	58.209
CEPAL Full Adder type 2	0.09796	0.0169	49.247

Fig. 6. Proposed Array multiplier implementation using CEPAL adiabatic logic.

Table 3. Power and energy analysis of Multiplier using the proposed adder

Circuit	Power clock= 1GHZ			
	P_{avg} (µW)	Iavg (nA)	(Tstop-Tstart) (S)	E (fJ)
CEPAL proposed 4X4 VEDIC MULTIPLIER	3.8816	502.9	9.99E-07	1938.9
CEPAL proposed 4X4 ARRAY MULTIPLIER	0.00705	5.2618	9.99E-07	3.5875