

## AN OVERVIEW OF THE SOLUTIONS FOR THE IMPLEMENTATION OF ASYNCHRONOUS DIGITAL SYSTEMS

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**Abstract:** A variety of solutions for the implementation of asynchronous digital systems have been described in the literature. This paper presents several implementation methods of these systems, including self timed circuits, speed independent circuits, delay insensitive circuits, handshake protocol, and C Muller elements. We also describe an implementation case study. Using the predefined circuits models in implementation of asynchronous digital systems means avoid errors and digital hazard situations. The digital asynchronous system will run correctly, according with the specifications.

**Keywords** Asynchronous digital systems, self timed, speed independent, delay insensitive, handshake, logic gates, asynchronous digital sequential system, C Muller elements.

### 1. INTRODUCTION

This paper is an overview for the methods of implementation of the asynchronous digital systems using self timed, speed independent, delay insensitive circuits, handshake protocol, and C Muller element.

A delay insensitive circuit works correctly indifferent of the propagation timing delays through wires and circuits. A speed independent circuit works correct rather than the propagation timing delays through circuits. Our assumption is that wires has a specific delay propagation values.

A self timed circuit uses delay elements where the wires delay propagation timing are known or negligible. Using the time information values, they are build like speed independent circuits.

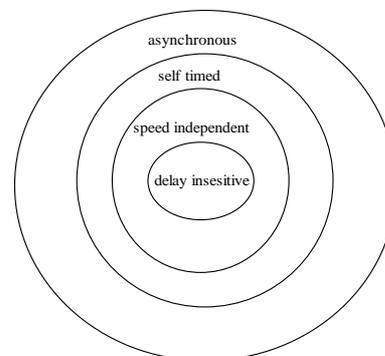


Fig.1. Implementation methods

The asynchronous sequential systems represents the general category, they haven't a locally clock signal, they are running using internally timing values. The latches and flip-flops circuits works asynchronous, they have the time set-up and time-hold predefined values.

Figure 1 presents the taxonomy of the implementation methods for asynchronous digital systems.

## 2. DATA COMMUNICATION

When two digital systems communicate, the receiver system must know when the data is valid, (Jennings et al.,1996). In asynchronous digital systems, the receiver must be triggered by the sender when the transmission of data starts or ends. This is done using the ACK signal (acknowledge signal). The active system block initiate the communications and the passive system block responds to the actions initiating by the active system block, (Oliveira et al.,2012). The concept used in the design of the asynchronous digital systems is named handshake, (Aghion et al., 2013), fig 2.

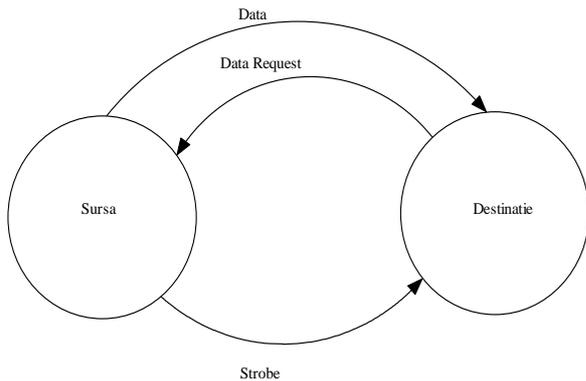


Fig.2. Communication – handshake protocol

The data transfer is starting by the sender by activation of the Data and Strobe signals, the acknowledge process is done by the receiver when the Data Request signal is generated, fig. 3.

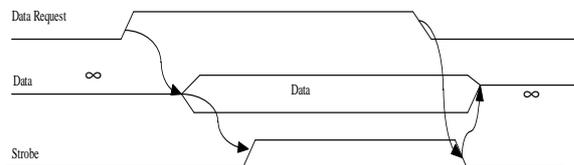


Fig.3. Communication – handshake protocol waves

In asynchronous digital systems there are no differences between level and edge signal transitions, see fig. 4.

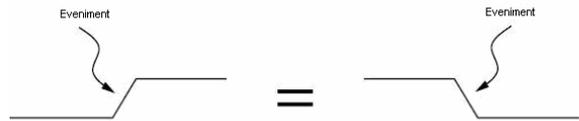


Fig.4. Signals – level vs edge events

## 3. CIRCUIT MODELS.

A completed digital circuit represents a system with two parts: the digital circuit and the system's environments where it runs. A digital circuit model describes how the logic gates delays are displayed.

There are two delay types: stray delay which inherit the physical properties of any circuits, and delay elements which are added by the designers.

The delay elements can be classified in pure delays and inertial delays. The pure delays propagates the signal from the output after a fixed time period, noted with  $d$ , fig. 5. The pure delays can be implemented using buffers.

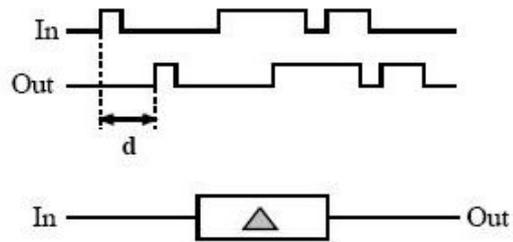


Fig.5. Delay elements

The inertial delays propagates only the signals which are stable for a period of time, (Reinhardt et al., 2005), these are delayed with a fixed time noted with  $d$ . Inertial delays are used for the glitch free filtering, fig. 6.

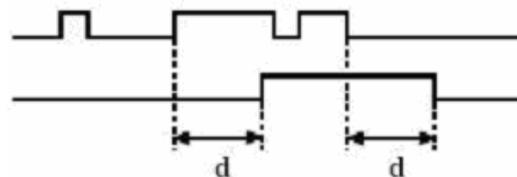


Fig.6. Inertial delay waves

The delays generated by the wire delays are implemented in the circuit's inputs. The gate delays are represented on the output of the circuits. The circuits that uses delays in the inputs and outputs are the most difficult to be implemented, fig.7.

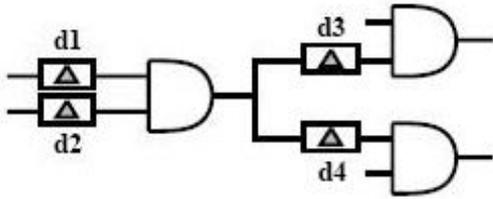


Fig.7. Wire delays

3.1. C Muller Elements

A delay insensitive circuit have arbitrary delays for wires or logic gates. A delay insensitive circuit has module blocks and the interconnection between them. Every module block must be designed to not influence the stability of the entire digital system. The hardware logic design can be complex to do because of the acknowledge ACK signal

In this case is much better to use the Muller C logic gate, fig. 8.

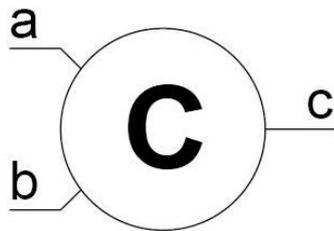


Fig.8. C Muller symbol element

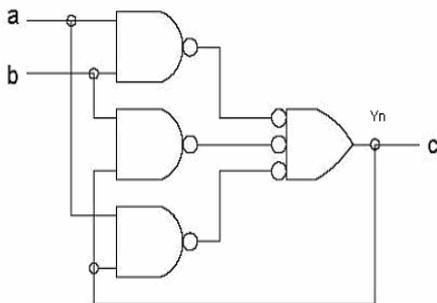


Fig.9. C Muller logic gates internal implementation

The equation for the C Muller logic gate is

$$(1) \quad c = \bar{a}bc_{n-1} + \bar{a}b\bar{c}_{n-1} + ab$$

With the notation  $c=y_{n+1}$ , the C Muller logic gate equation becomes:

$$(2) \quad y_{n+1} = \bar{a}by_n + \bar{a}b\bar{y}_n + ab$$

And the resulting truth table is shown in Table 1.

Table 1 C Muller Truth Table

a b	$y_n$	$y_{n+1}$
0 0	-	0
0 1	-	$y_n$
1 0	-	$y_n$
1 1	-	1

4. CASE STUDY. SYNTHESIS OF AN ASYNCHRONOUS DIGITAL SYSTEM USING LOCALLY CLOCK METHOD

The implementation of the asynchronous digital systems using locally clock was described by (Nagy, et al.,2014; Garcia, et al., 2014).

The locally clock signal depends by the system's states notated with  $Q_i$ , input signals notated with  $X_j$ , where  $i=1,2,\dots,n-1$ ,  $j=1,2,\dots,m-1$ ; ( $n$  represents the states variables number,  $m$  represents the input variables number).

If clock signal  $CK=1$  the system will go onto a new state, if  $CK=0$  the system will stay in present state, it will can read the output values signals. While the states and output signals are computed, the input signals will not be changed, the system will work in fundamental mode, (Timis et al., 2007).

Let's consider the graph algorithm description of a digital system, fig.10.

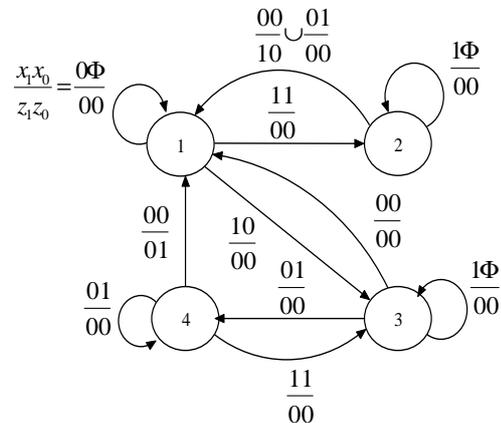


Fig. 10. Graph algorithm

The system's equations are described in (3):

$$D_1 = y_{1,n+1} = [y_1(x_0 + x_1) + \bar{y}_0\bar{x}_1\bar{x}_0]_n$$

$$(3) \quad D_0 = y_{0,n+1} = x_{1,n}$$

$$z_{1,n} = (\bar{y}_1\bar{y}_0\bar{x}_1\bar{x}_0)_n$$

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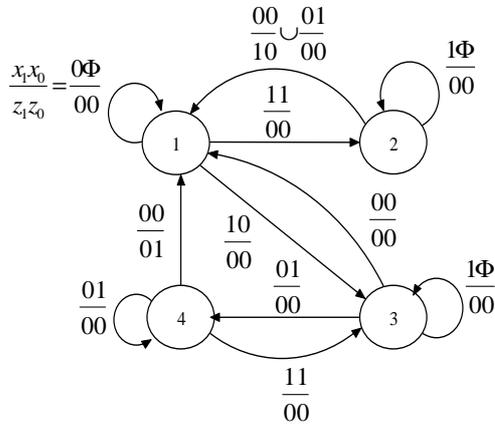


Fig.10. Graph algorithm

The system's equations are described in the equations (3-6):

$$(3) D_1 = y_{1,n+1} = [y_1(x_0 + x_1) + \overline{y_0}x_1\overline{x_0}]_n$$

$$(4) D_0 = y_{0,n+1} = x_{1,n}$$

$$(5) z_{1,n} = (\overline{y_1}y_0\overline{x_1}x_0)_n$$

$$(6) z_{0,n} = (\overline{y_1}y_0x_0)_n$$

The implementation of the asynchronous system, using D latch is presented in fig.11.

Using the Veitch-Karnaugh logic minimization method it will be computed the CK's equation, (7):

$$(7) CK = \overline{x_1}y_0 + x_1\overline{y_0} + \overline{x_0}y_1\overline{y_0}$$

After computing the timing for the entire system, we get the value:  $\Phi = 313.6ns$ .

In this way, the system works faster and the possibility of logic hazard are eliminated.

If the delay from Q signal to the Res signal has value  $\Phi = 314ns$ , the entire asynchronous system will work correctly, (Timis et al., 2007).

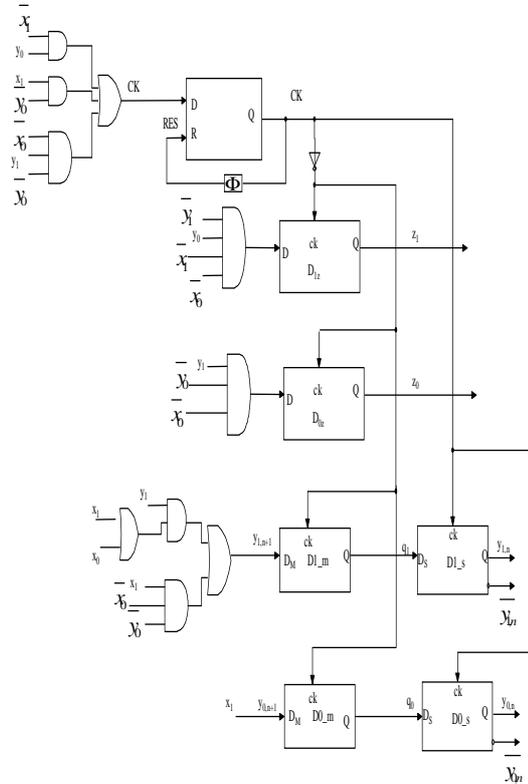


Fig.11. Implementation using D latches

## 5. CONCLUSIONS

The delay insensitive circuits are used as control circuits. A different delay model is represented by the speed independent circuits. It counts only the delays through logic gates, the wire delays aren't taken into account. A speed independent circuit run good indifferent by the delays through logic gates. The bounded delay means that the delay for every logic gate must be less than a maximum set value. This model is common used in digital asynchronous systems. Using the predefined circuits models in the implementation of asynchronous digital systems allows the avoidance of errors and digital hazard situations. The digital asynchronous system will run correctly, according with the specifications.

In our case study, the minimum propagation delay of CK signal through the combinational system must be greater than the maximum propagation delay for every logic circuit which implements the input/output signals, thus the entire asynchronous digital system will operate in accordance with the specifications

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