THE ANNALS OF "DUNAREA DE JOS" UNIVERSITY OF GALATI
FASCICLE III, 2010, Vol.33, No.2, ISSN 1221-454X
ELECTROTECHNICS, ELECTRONICS, AUTOMATIC CONTROL, INFORMATICS

ATMEL MICROCONTROLLER BASED SOFT SWITCHED PWM ZVS FULL BRIDGE DC TO DC CONVERTER

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Abstract: This paper deals with the simulation and implementation of soft switched PWM ZVS full bridge DC to DC converter. The 48V DC is efficiently reduced to 12V DC using a DC to DC converter. This converter has advantages like reduced switching losses, stresses and EMI. Input DC is converted into high frequency AC and it is stepped down to 12V level. Later it is rectified using a full wave rectifier. Laboratory model of microcontroller based DC to DC converter is fabricated and tested. The experimental results are compared with the simulation results.

Keywords: DC-DC converter, full bridge converter, soft–switching, zero voltage switching (ZVS)

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1. INTRODUCTION

Voltage-source pulse-width modulation (PWM) inverters have been widely used in industrial application such as uninterruptible power supplies. The harmonics can be easily eliminated by power filter and it has a capability in allowing continuous and linear control of the frequency and fundamental component of the output voltage. However, for increase in power density, it must increase the switching frequency to reduce the size and weight of components. Even if the increased switching frequency does not cause unacceptable switching losses, the oscillations caused by converter parasitic elements may cause high current and voltage stresses, which are almost unpredictable, depending on circuit layout. Suitable snubber circuits must therefore be adopted, which affect power density and converter reliability. The research and application of zero-voltage switching (ZVS) is gaining increasing attention, as this converter family promise to combine the simplicity of PWM converters with the soft switching characteristics of resonant converters

The phase-shifted PWM full bridge (FB) converter incorporates the leakage inductance of the transformer to achieve Zero-voltage switching (ZVS) of the primary switches. The elimination of the need for the primary side snubbers enable high frequency power conversion for high input voltage and high power applications. As a result, the power density and the efficiency of the converter can be improved. However, when ZVS is required over a wide load and/or line range, the leakage inductance is deliberately increased and/or a large external resonant inductor is added, resulting in an excessive duty cycle loss and very severe secondary side parasitic oscillations. This increases the primary side conduction losses and the secondary side snubber

This paper was recommended for publication by Marian Gaiceanu

losses, and therefore decreases the efficiency of the converter.

Several new techniques for high frequency DC-DC conversion are there to reduce component stresses and switching losses while achieving high power density and improved performance. Among them, the full-bridge (FB) zero-voltage-switched (ZVS) converter is one of the most attractive techniques which is shown in Fig. 1. It is the most widely used soft-switched circuit in high-power applications, (Redl, *et al.*, 1991; Sabate, *et al.*, 1991; Chen, *et al.*, 1995). This constant-frequency converter employs phase-shift (PS) control and features ZVS of the primary switches with relatively small circulating energy. In this technique a control circuit serves to supply pulsed control signals Q_1 to Q_4 to the switching transistors of the converter for maintaining the output voltage at its desired level using phase shift control in known manner. The signals Q_1 and Q_2 are generally complementary to one another at a desired switching frequency, and the signals Q_3 and Q_4 are relatively variably phase shifted from the signals Q_1 and Q_2 to provide the phase shift control. With no phase-shift between the legs of the bridge, no voltage is applied across the primary of the transformer. So, the output voltage is zero. Similarly if the phase shift is 180^0, maximum voltage is applied across the primary winding, which produces the maximum output voltage. ZVS of the lagging-leg switches Q_1 and Q_2 is achieved primarily by the energy stored in output filter inductor L1. Since the inductance of L1 is large, the energy stored in it is sufficient to complete discharge parasitic capacitances C_1 and C_2 of Q_1 and Q_2 to achieve ZVS. But the discharge of parasitic capacitances C_3 and C_4 of leading-leg switches Q_3 and Q_4 is done by leakage inductance L of the transformer which is small. The ZVS range of the leading-leg switches can be extended by intentionally increasing the leakage inductance of the transformer and/or by adding a large external inductance in series with the primary of the transformer. This increased inductance has a detrimental effect on the performance of the converter since it causes an increased loss of the duty cycle on the secondary side, as well as severe voltage ringing across the secondary-side output rectifiers due to the resonance between the inductance and the junction capacitance of the rectifier. The secondary-side ringing can be suppressed by an active snubber described in (Sabate, *et al.*, 1991).For implementations with an external primary inductor, the ringing can also be effectively controlled by employing primary-side clamp diodes D_1 and D_2 as shown in Fig. 1, as proposed in (Redl, *et al.*, 1991). Though the snubber approaches in (Redl, *et al.*, 1991; Sabate, *et al.*, 1991) offer practical and efficient solutions to the secondary-side ringing problem, they do not offer any improvement of the secondary-side duty-cycle loss.

Several techniques have been proposed to extend the ZVS range of FB ZVS converters without the loss of duty cycle and secondary-side ringing (Jain, *et al.*, 2002;Ayyanar,and Mohan,2001; Mason,and Jain,2005; Jang, and Jovanovic,2004). Generally, these circuits utilize energy stored in the inductive components of an auxiliary circuit to achieve ZVS for all primary switches in an extended load and input voltage range. Ideally, the auxiliary circuit needs to provide very little energy, if any, at full load because the full-load current stores enough energy in the converter's inductive components to achieve complete ZVS for all switches. As the load current decreases, the energy provided by the auxiliary circuit must increase to maintain ZVS, with the maximum energy required at no load. The energy stored for ZVS is independent of load as described in (Jain, *et al.*, 2002; Ayyanar,and Mohan,2001). Adaptive energy storage in the auxiliary circuit has been given in Mason,and Jain,2005; Jang, and Jovanovic,2004). However, these converters have to use large inductors so; high circulating energy is needed to achieve no-load ZVS.

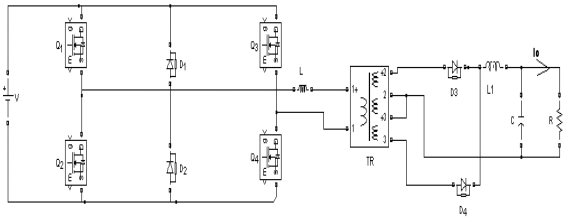

Fig.1. PWM Full Bridge Converter

In this paper, a FB ZVS converter with adaptive energy storage that offers ZVS of the primary switches over a wide load range with greatly reduced no-load circulating energy and with significantly reduced secondary-side duty cycle loss is introduced with PWM control. ZVS full bridge DC to DC converter with ZVS over the entire range is given by (Mangesh Borage, *et al.*, 2008). High power density multikilowatt DC to DC converter with galvanic isolation is given by (Martin Pavlovsky, *et al.*, 2009). All the referred literature listed does not deal with embedded implementation of PWM ZVS full bridge converter. This work aims to implement ZVS full bridge converter using Atmel microcontroller. The operational principle, simulation results, and experimental results are presented to confirm the validity of the converter operation.

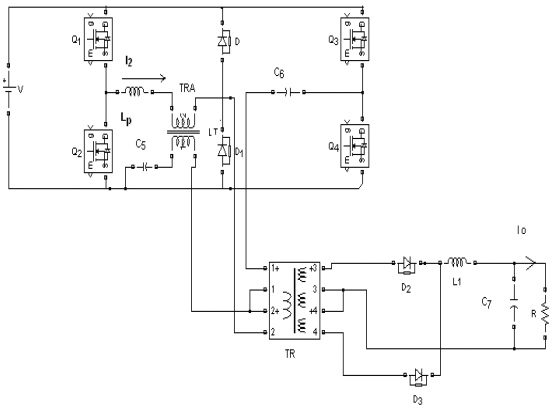

Fig. 2 Modified FB ZVS converter

Technical Specifications of Fig. 2:

DC input voltage=48V,Lp=0.01µH, R=25Ω, L1=28µH,C7=120µF,C5=0.5µF,C6=12µF,
Operating frequency =20 KHz.

In the modified circuit, since the ZVS energy stored in the primary inductor is dependent on its inductance value and the volt-second product of the secondary of auxiliary transformer TRA, the size of the primary inductor can be minimized by properly selecting the turns ratio of auxiliary transformer TRA. As a result, the size of the primary inductor is very much reduced compared to that of the conventional PS FB converter shown in Fig. 1. In addition, since the auxiliary transformer does not need to store energy, its size can be small. Finally, because the energy used to create the ZVS condition at light loads is not stored in the leakage inductances of transformer TR, the transformer's leakage inductances can also be minimized. As a result of the reduced total primary inductance, i.e., the inductance of the primary inductor used for ZVS energy storage and the leakage inductance of the power transformer, the modified converter exhibits a relatively small duty-cycle loss. This minimizes both the conduction loss of the primary switches and the voltage stress on the components on the secondary side of the transformer, which improves the conversion efficiency. Moreover, because of the reduced total primary inductance, the secondary side parasitic ringing is also reduced and is effectively controlled by primary side diodes D and D_1.

2. OPERATIONAL PRINCIPLE

The circuit diagram of the modified converter is shown in Fig.2.The primary side consists of four switches, two diodes, one inductor, and one capacitor. It employs low power auxiliary transformer TRA to extend the ZVS range. At light loads energy used to create ZVS is not stored in the leakage inductance of the transformer TR .So, the transformer's leakage inductance can be minimized. Energy stored in primary inductor depends on volt-second product of the secondary of auxiliary transformer TRA and inductance value. Therefore by selecting proper turn ratio of auxiliary transformer TRA, the size of the primary inductor can be minimized. Auxiliary transformer is not used to store energy. So, its size can be small. Several assumptions are made as follows.

1. Capacitance of capacitor C_5 is large enough so that the capacitor can be modeled as a constant voltage source.
2. The inductance of output filter L1 is large enough so that during a switching cycle the output filter can be modeled as a constant current source.
3. The leakage inductance of auxiliary transformer TRA and the magnetizing inductances of both transformers are neglected.
4. The resistance of each conducting switch is zero, whereas the resistance of each non-conducting switch is infinite.
5. Current through primary side of auxiliary transformer TRA is zero.

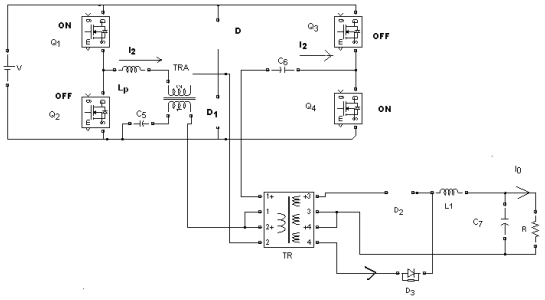

Fig. 3(a) The circuit diagram at (t_0 to t_1)

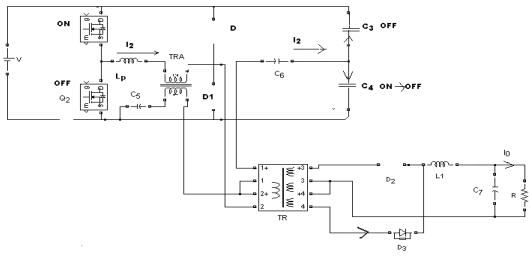

Fig. 3(b) The circuit diagram at (t_1 to t_2)

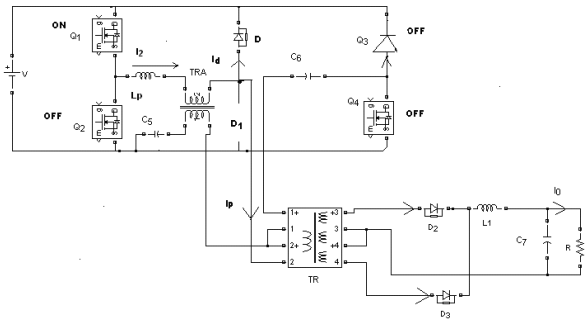

Fig. 3(c) The circuit diagram at (t_2 to t_3)

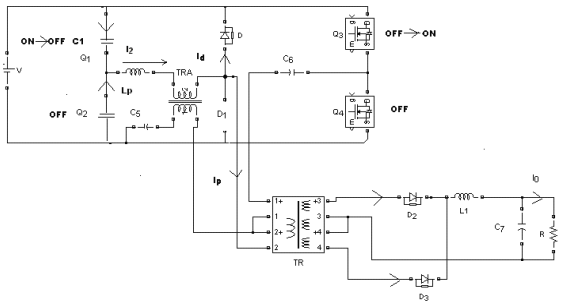

Fig. 3(d) The circuit diagram at (t_3 to t_4)

As shown in Fig,3(a), at $t=t_0$, load current flows through rectifier D_3 and the lower secondary of power transformer TR, when diagonal switches Q_1 and Q_4 are conducting. Since during this topological stage diodes D and D_1 are reverse biased, the reflected primary current flows through closed switch Q_1, primary inductor L_p, winding N_2 of auxiliary transformer TRA, primary winding N_p of transformer TR, and closed switch Q_4. The impendence of the primary inductor Lp and winding N_2 of auxiliary transformer TRA are very small compared to primary referred filter inductor L_o' .Let V_o' is the primary referred output DC voltage.

Slope of the primary current is given by $(V_{DC} - V_o')/ L_o'$. Centre tap of primary voltage is given by $V_P/2 = V/2$ because impendence of primary inductor Lp and winding N_2 of TRA are small. At $t=t_1$ as shown in Fig. 3(b), switch Q_4 is turned off, primary current starts charging output capacitance C_4 of switch Q_4 and discharges output capacitance C_3 of switch Q_3. The total required energy to charge C_4 and discharge C_3 is provided not only from the stored energy of L_p, but also from the stored energy of the output filter inductor. Since the stored energy in the output filter inductor is significantly larger than the required energy to charge C_4 and discharge C_3, these capacitors are assumed to be charged and discharged linearly. Voltage across switch Q_4 increases towards V and voltage across switch Q_3 decreases towards zero. Primary winding voltage of auxiliary transformer increases from zero to V/2 and secondary winding of auxiliary transformer increases from zero to V/2ni, where ni is the auxiliary transformer turn ratio. Diode D starts conducting because of the increasing secondary voltage of the auxiliary transformer. After voltage across Q_3 reaches zero, diode across Q_3 starts conducting at $t=t_2$ as shown in Fig. 3(c).

When the voltage across switch Q_3 becomes zero, voltage across the power transformer also becomes zero, since the primary of the transformer is shorted by the simultaneous conduction of the body diode of Q_3 and diode D. As a result, the secondary windings are also shorted so that rectifiers D_2 and D_3 can conduct the load current simultaneously. However, because of the leakage inductance of transformer TR, load current I_o is still carried by the lower secondary through rectifier D_3 since no voltage is available to commutate the current from the lower secondary and D_3 to the upper secondary and D_2 if ideal components are assumed. With real components this commutation voltage exists, but is too small to commutate a significant amount of current from the lower to the upper secondary so that even with real components the majority of the current is still found in the lower secondary and its corresponding rectifier D_3. So, during this stage when switches Q_1 and Q_3 are conducting, primary current stays nearly unchanged.

During this stage, diode D is conducting and voltage V_2 is applied directly across primary inductor L_p, which increases current I_2 until Q_1 is turned off at $t=t_3$ as shown in Fig 3(d).Current $I_2(t)$ in the interval of t_2 to t_3 can be given as

(1) $I_2(t) = I_p + I_d(t) = I_o/n + \{V/ 2niLp(t-t_2)\}$

Where $I_d(t)$ is the current across diode D.
n=turn ratio of power transformer.

During this stage, the voltage across switch Q_3 is kept zero due to D. So switch Q_3 is turned on with ZVS. After Q_1 is turned off, current I_2 begins charging output capacitance C_1 of switch Q_1 and discharging capacitance C_2 of switch Q_2.The total energy required to charge C_1 and discharge C_2 is supplied from the stored energy in the primary inductor L_p. To achieve ZVS energy stored in the primary inductor (E_{LP}) must be higher than total energy required to charge C_1 and discharge C_2.

(2) $E_{LP} \geq CV^2$

Where $C_1 = C_2 = C$
Using equation (1)

$$(3)\ E_{LP} = \frac{1}{2} L_P \left(\frac{I_o}{n} + \frac{V(1-D)}{4 n i L_P f_S} \right)^2$$

Where f_s is the switching frequency.

Then primary current continues to flow through antiparallel diode of switch Q_2 so that Q_2 can be turned on with ZVS.

In this stage Voltage V_{s1} across switch Q_1, which is in opposition to voltage V_2, starts increasing and current I_d starts decreasing. When I_d becomes zero, Diode D stops conducting so that the primary current starts decreasing. Load current I_0 also begins to commutate from the lower secondary and D_3 to upper secondary and D_2. When the commutation of the load current from the lower to upper secondary is completed, the primary current commutation from the positive to negative direction is also finished.

The circuit stays with diagonal switches Q_2 and Q_3 turned on until switch Q_3 is turned off. Second half of the switching period is exactly the same as the first half of the switching period.

3. SIMULATION RESULTS

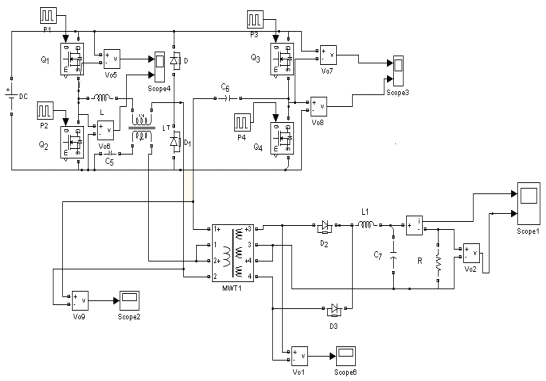

Fig.4 Simulink Model Of ZVS DC to DC converter

The ZVS DC to DC converter is simulated using Matlab Simulink and the results are presented here. Simulink model of DC to DC converter is shown in Fig 4. Driving pulses are shown in Fig. 5.DC input voltage is shown in Fig 6.Output voltage across Q_1 & Q_2 is shown in Fig 7.Voltage across Q_3 & Q_4 are shown in Fig 8. .Secondary voltage is shown in Fig 9. DC output current and voltage are shown in Fig. 10. DC output voltage is 12V and the current is 1A. It can be seen that the DC output is free from ripple.

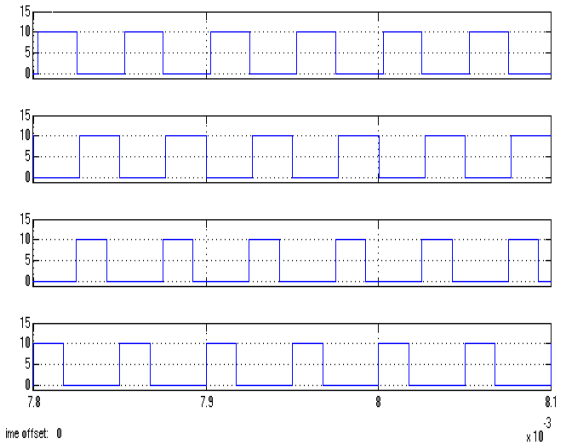

Fig.5 Driving Pulses

For constant-frequency, variable duty cycle control of the proposed converter, switches Q_1 and Q_2 always operate with approximately 50% duty cycle, whereas switches Q_3 and Q_4 have a duty cycle in the range from 0% to 50% as shown in Fig. 5.

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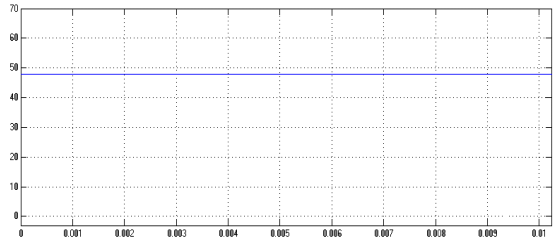

Fig.6 DC Input Voltage

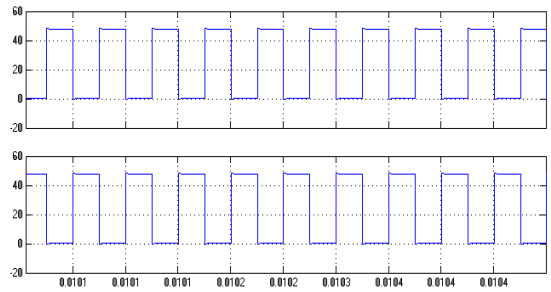

Fig.7 Output Voltage across Q_1 and Q_2

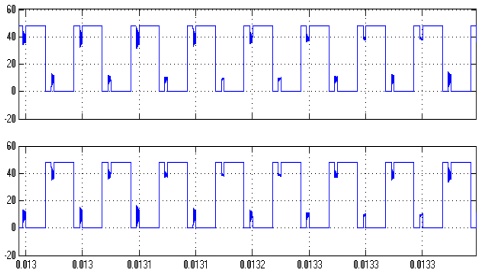

Fig.8 Output voltage across Q_3 and Q_4

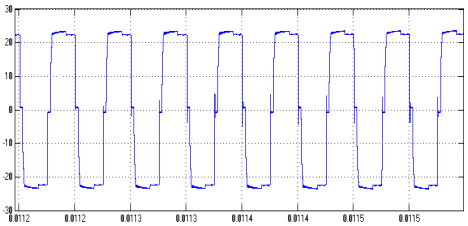

Fig. 9 Voltage across the secondary

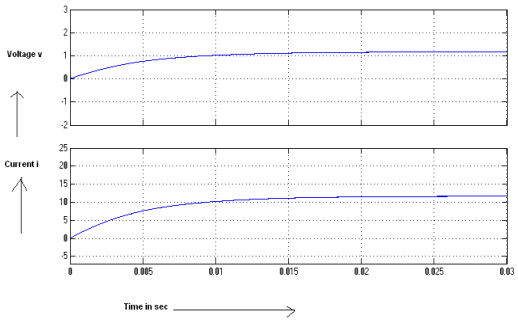

Fig.10 DC output current and voltage

Table1 shows the performance of modified FB ZVS converter. Table2 shows the performance of conventional FB converter. A comparison of the performance of the modified FB ZVS converter and conventional FB converter is presented in table3.For conventional FB converter and modified FB ZVS converter Fig.11 shows the dependence of output voltage versus load resistance, Fig12 shows variation of output power with the variation in load resistance, Fig13 shows the variation of output power with input power, and Fig.14 shows the variation of efficiency with load resistance.

Table1.Performance of modified FB ZVS converter

Load resistance	Input power	Output power	Output voltage	Output current	Efficiency
5	30.81	27.0789	9.34	2.899	87.89
10	21.69	19.011	9.73	1.9538	87.65
15	17.85	15.5562	10.12	1.5371	87.15
20	15.4	13.322	11.25	1.1841	86.51
25	13.68	11.7497	12.21	0.9623	85.89
30	12.4	10.5412	12.85	0.82032	85.01

Table2. Performance of conventional FB converter

Load resistance	Input Power	Output power	Output voltage	Output current	Efficiency
5	30.81	25.831	9.3	2.777	83.84
10	21.69	18.106	10.02	1.806	83.48
15	17.85	14.795	10.85	1.3635	82.89
20	15.4	12.738	11.79	1.08	82.72
25	13.68	11.171	12.64	0.883	81.66
30	12.4	10.034	13.01	0.771	80.92

Table3. Performance comparison

Load resistance	Efficiency conventional	Efficiency modified
5	83.84	87.89
10	83.48	87.65
15	82.89	87.15
20	82.72	86.51
25	81.66	85.89
30	80.92	85.01

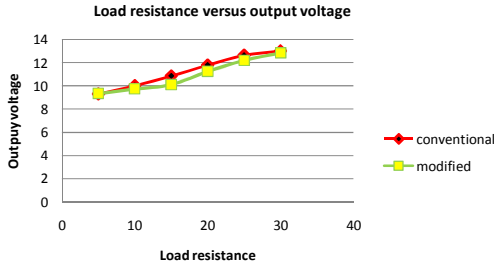

Fig.11 output voltage versus load resistance

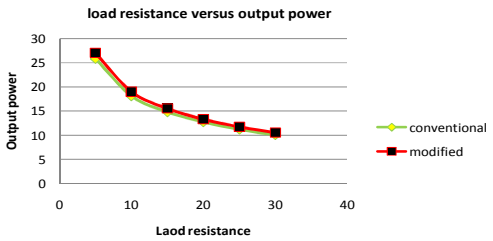

Fig.12 output power versus load resistance

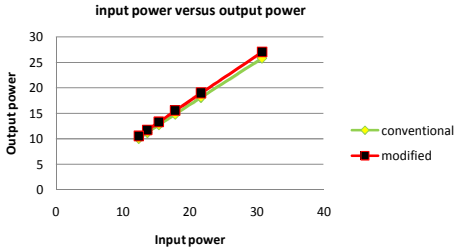

Fig. 13 output power versus input power

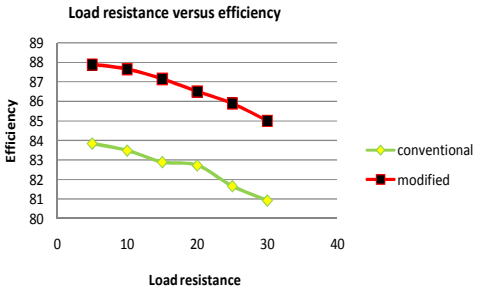

Fig.14 efficiency versus load resistance

4. **EXPERIMENTAL VERIFICATION**

The DC to DC converter was built and tested at 48V DC. The circuit parameters are as follows. The hardware layout is shown in Fig.15.

R=25Ω,C7=100μF,L1=28mH,L_p=0.02mH,and the switching frequency is 20 kHz. Experimental waveform of voltage across the primary is shown in Fig.16, voltage across the secondary is shown in Fig.17 and output voltage is shown in Fig. 18.

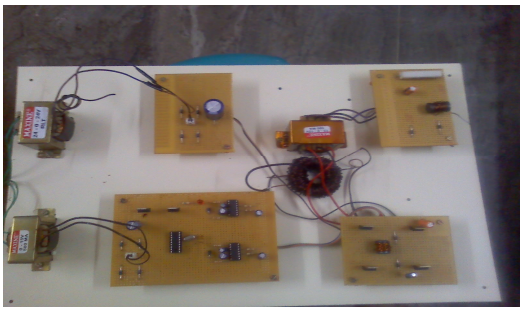

Fig. 15 Hardware Layout

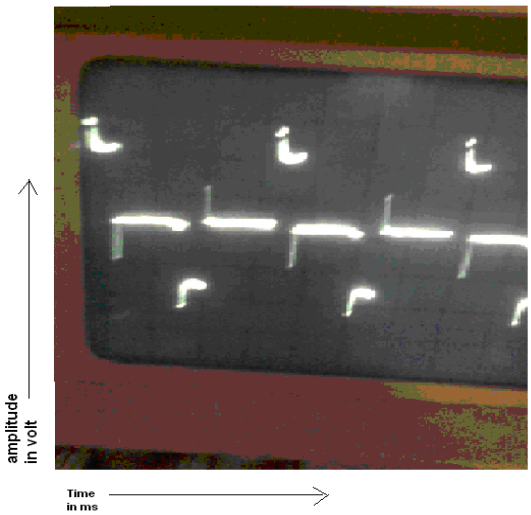

Fig. 16 Voltage across the primary

X axis 1 div=0.5ms, Y axis 1div=20V.

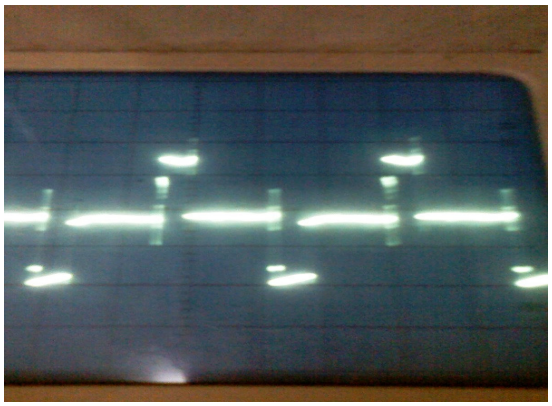

Fig.17 Voltage across the secondary

X axis 1 div=0.5ms, Y axis 1div=20V.

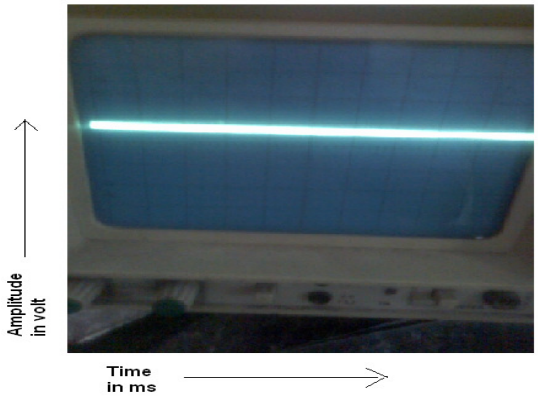

Fig. 18 Output voltage

X axis 1 div=0.5ms, Y axis 1div=10V.

5. CONCLUSION

ZVS DC to DC converter is modeled using the blocks of simulink. Soft switched ZVS PWM DC to DC Converter is analysed, simulated , tested and the results are presented. Conversion from 48V DC to 12V DC is done using soft switched PWM converter. Switching losses and stresses are reduced using zero voltage switching.. This converter can be used for battery charging and Electrolysis. The scope of this work is the modeling, simulation and testing of ZVS DC to DC converter. The experimental results closely agree with the simulation results.

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