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A SIMPLE LOAD POWER ESTIMATOR FOR QUASI-DIRECT AC-AC CONVERTER SYSTEM.

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Abstract: In this paper a simple load power estimator for the three-phase quasi-direct ac-ac converter system is reported. Since the ac-ac converter control by means of pulse-width modulation (PWM) is based on the power balance concept, its load power should be known. Two control boards, based on the dSMC (digital Smart Motion Controller) 30 MIPS 32-bit fixed-point digital signal processor (DSP), were involved in the ac-ac system driving. By using the power balance control, the DC link voltage variation at the load changes can be reduced. In this way a small DC link capacitor is required to handle the dc voltage error control. The feed-forward (Sul and Lipo, 1990) current component provides fast correction of the reference control to load power variation. In order to obtain the feed-forward current component, the load power must to be known. In this paper the load power is estimated from the dc link, indirectly, through a dc load current estimator. In this way the author overcomes the use of the serial communication between control boards (Gaiceanu, 2004) in order to deliver the load power information from the inverter side. The load current estimator is based on the DC link voltage and on the load current of the supply converter. This method presents certain advantages instead of using measured method, which requires a low pass filter: no time delay, the feed-forward current component has no ripple, no additional hardware, and more fast control response. Through simulation and experimental results the performances of the proposed load current estimator scheme are demonstrated.

Keywords: current estimator, PWM ac-ac converter, power balance, load feed-forward, digital control, synchronous current controller, rotor field oriented control.

1. INTRODUCTION

In this paper the topology of the 37 kW ac-ac prototype, the detailed dc load power estimator and the experimental results are provided. In order to apply power balance control, the output power of the ac-ac system should be known. Many authors deliver different methods to obtain load power information. One of these methods is to measure (Wu, *et al.*, 1990; Malesani, *et al.*, 1995; Singh, *et al.*, 1999) the power supplied from the inverter and to use a low pass filter. This method has as consequences in time delays in the current control. Another method is to estimate (Kim, and Sul,1993;Habetler, 1993)) the load power. The load power can be estimated from the inverter side or dc side. In the dc side case, the dc link current measurement becomes a serious problem at large inverter power rating due to the stray inductance of the bus bar system between capacitors and insulated gate bipolar transistors (Ziogas, *et al.,* 1985). The output power estimator used in the load feed-forward loop provides the current output, I^*_{q2} (Fig.2). The load feed-forward current converter was

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introduced to force the converter power to match the power (Ooi, *et al.,* 1988) required by the inverter. The use of load feed-forward increases the dynamic response of the dc link voltage to load changes.

2. SYSTEM DESCRIPTION

This section describes the power stage of the ac-ac converter, both control of the converter and inverter, and some design considerations.

2.1. The power stage.

The power stage is formed by two three phase IGBT power modules connected through the dc link capacitor, and input inductor.
The boost inductor limits the peak switching currents to an acceptable value and smooths the line currents. The DC link capacitor provides a decoupling function between the grid side and load side. The amount of the energy stored in the dc link capacitor is such that to maintain the dc link voltage ripple in a suitable limit. Thus, the dc link capacitor has two functions: to filter dc link voltage ripple and to store energy during the delay time of the dc link voltage loop.

2.2. The control stage.

Converter side:

The voltage regulation assures no error in power matching, acting as an outer loop of the system, and no steady-state error in dc link voltage at reference and load variations.

The power balance control assures a reduced ripple in dc link voltage, and thus a small dc link capacitor is used.

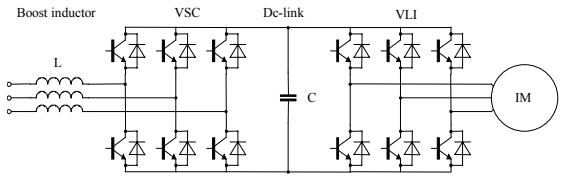

Fig. 1. The power stage of the three-phase ac-ac converter system (VSC- voltage source converter, VLI-voltage load inverter).

By synchronizing, through the current control, the phase angle of the current reference of the source converter with the phase of the utility voltage, the unity power factor is obtained. The currents in two phases at converter input are sensed (i_a and i_b) and, thereafter, current in the third phase, i_c, is derived (Fig.2). Through the Clarke and Park transformations, the feedback currents are provided.
A feed-forward power loop was introduced in order to have fast control of the active power to load changes. For the feed-forward power control (Fig. 2), DC link voltage is sensed and load current is estimated. Then, these signals are processed in the power estimator to make available its output I^*_{q2}, which is added to the PI voltage controller output, I^*_{q1} (Fig.2). Further, I^*_{q1} and I^*_{q2} together form the magnitude of the reference current, I^*_q (Fig.2). By using the synchronous rotating frame, the active and reactive power can be controlled independently by proportional-integral (PI) current controllers that ensure zero-steady state error. The current regulators generate the adequate switching states for the corresponding power converters entire the whole load range through the gate drives. IGBT gate drive boards are directly mounted around IGBT modules.
The phase-locked loop (PLL) is necessary for the proper current controllers decoupling, and for *d-q* axes synchronization with the grid reference voltage, respectively. The PLL tracks the grid frequency.

Inverter side:

In order to independently control the flux and the torque output for an induction motor, to meet field oriented control requirement, rotor flux should be aligned with the *d* axis. The measured speed, ω_r, is compared with the reference speed, ω^*_r, to decide the required torque of the induction motor (IM). The rotor flux regulator is a PI controller and therefore the steady state error between the rotor flux reference and the estimated rotor flux is zero. To incorporate the synchronous current regulators into indirect field oriented control (FOC), based on synchronously rotating *d-q* frame, the sensing stator currents (i_u, i_v) are transformed into complex state vectors ($i_{s\alpha}$, $i_{s\beta}$) based on stator coordinates through Clarke transformation, and in synchronous reference frame through the Park transformation, respectively.

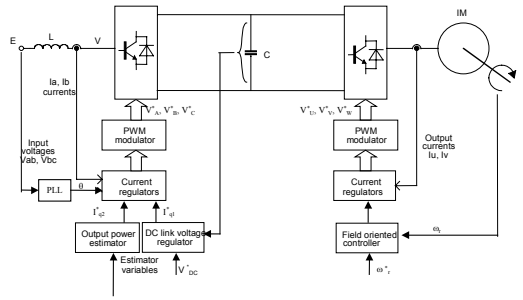

Fig. 2. Control block diagram of the AC-AC converter.

The current regulators process the input current errors and provide the synchronous references for the voltage inverter. The transformation between the rotationally coordinate and the stationary coordinated system is done through the inverse Park transformation. Applying two-phase to three-phase transformation, the voltage references (V^*_u, V^*_v and V^*_w) for the pulse width modulator inputs' are obtained.

The field-oriented controller contains speed, flux and indirect field oriented controllers. The indirect field oriented controller performs the field-oriented mechanism.

For the closed-loop control of the induction motor, its sensed speed is compared with the set reference speed. Speed error so obtained is processed in the PI speed controller. The output of the speed controller is the reference torque. The reference magnetizing current vector is worked out in the field-weakening block (not represented in Fig.2).

By comparing the reference currents (I^*_{sd} and I^*_{sq}) with the feedback currents (I_{sd}, I_{sq}), the corresponding current errors are processing in PI current regulators in order to deliver the reference voltages for the pulsewidth modulator (PWM). The *d*, *q* reference voltage outputs of the current regulators are converted to the stationary three-phase variables and then compared with the triangular wave form to extract the switch gate signals.

2.3. Design aspects:

The power stage

The input boost inductor is designed from the current THD factor constraint such that to be less than 5% at the full load. The dc link design is carried out under the assumption that the ripple current generated by the supply converter and load converter are equal in magnitude and are phase shifted by 180^o. In Fig. 1 is shown the power stage of the three-phase voltage ac-ac converter system. It contains two Semikron three-phase IGBT power modules, one three-phase boost inductor, and a 1000μF capacitor bank.

The power design of converters is affected by supply conditions to be sustained at rated power (IEC22G-WG4(cv)23B draft) (Fratta, *et al.*). Parameters for rated power design of converters are shown in the Table I.

Table 1 The main design parameters.

Parameter	Worst-case
Steady-state supply voltage	±10%
Frequency	±2%
Voltage unbalance	1%
Input current THD	<5%
DC ripple voltage	<5%

The control stage

Because in ac drive systems the performances are based only upon the equivalent small time constants of the control loops, by estimating the delay time of each loop and by knowing the switch frequency, the control bandwidth and PI control parameters are derived.

The bandwidths of the current and voltage sensors do not affect the system stability, since they are wider than the control bandwidth.
The digital filter bandwidth of the ac current signal is designed equal to the control bandwidth such that, the low pass filter has unity gain in the band of the control loop, i.e. must to have reduced gain at the switching frequency.

To avoid the aliasing effect in the analog to digital conversion system (ADC) a low-pass analog filter was placed to each input of the ADC. The filter's cut-off frequency should be below the Nyquist frequency of the system and above the input signal's frequency. According to the Nyquist rule, the minimum sample rate required to describe the signal is at least two times the highest system frequency. A second order Butterworth filter is used (Jones, 1995).

The block control diagram of the ac-ac system is shown in Fig. 2.
Each one of these loops is modeled separately and then joined together to have the complete model of the proposed drive system.
Assumption considerations for system modeling: the ac source voltages are balanced and distortion free, the converter switches are ideal, the DC voltage reference is constant, the load is balanced with a 0,96 inductive power load.

3. CONTROL OF THE VOLTAGE SOURCE CONVERTER

The detailed design methodology for the ac-ac converter system regulators is presented in (Gaiceanu, 2004).
In AC drive a unity power factor is necessary. This implies a proper orientation of the reference frame and a zero reference value for d-axis line current, I_d:

$$(1)\ I^*_d = 0$$

Low overshoot and fast response are the design criteria.

3.1. Voltage controller

By model linearizing through the small perturbation method around the equilibrium point the parameters of the dc-voltage controller were derived (Gaiceanu, 2004). The main task of the voltage controller is to maintain the dc link voltage to a certain value. Another task is to control the voltage converter power flow.

3.2. Current controllers

The internal (current) loops with wide bandwidth are needed to regulate the reactive power in order to achieve unity power factor, and to regulate the active power such that low dc voltage variation is ensured.

At the same time, the ac input current is regulated to be sinusoidal. The proportional integral (PI) controllers were used (Gaiceanu, 2004).
By using a decoupling method the cross coupling between the *d* and *q* axes due to boost inductance was compensated. Thus, by decoupling the *d* and *q* axes of the synchronous reference frame model, the first order current control loop plant is obtained.
The feed-forward current component was added to the reference. Their value is provided from the power balance equation, i.e. the power converter must meet the load power requirements. Therefore,

$$(2)\ I_{q2}^{*} = k_p \cdot \hat{P}_{out}$$

in which the proportional constant (considering that the supply voltage has the constant value) is given by:

$$(3)\ k_p = \frac{2}{3E}$$

Through the feed-forward component the power flow is controlled indirectly by the reference current.
The output dc link power is estimated as:

$$(4)\ \hat{P}_{out} = V_{dc}\hat{I}_{dcout}$$

The estimated dc link current is given by:

$$(5)\ \hat{I}_{dc} = I_{dcin} - \hat{I}_{dcout}$$

4. THE FIRST ORDER DC LOAD POWER ESTIMATOR

The block diagram of the first order estimator is presented in Fig. 3, where the input needs the measure of the dc link voltage $V_{dc}(p)$ and the calculus of the dc input current component I_{dcin}. The output of the estimator is the estimated dc load power $\hat{P}_{dcout}(p)$. It could be noted that the load power is estimated from the dc link, indirectly, through a dc load current estimator.

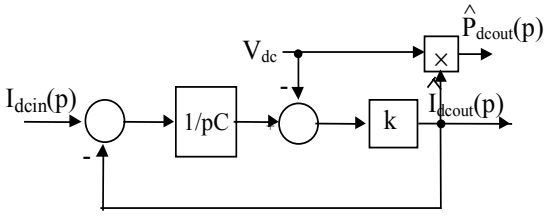

Fig. 3. The first order dc load power estimator.

After some manipulations the first degree estimator can be reduced as in Fig. 4.
Using Laplace transform the dc link equation becomes:

$$(6)\ pCV_{dc}(p) = I_{dcin}(p) - I_{dcout}(p)$$

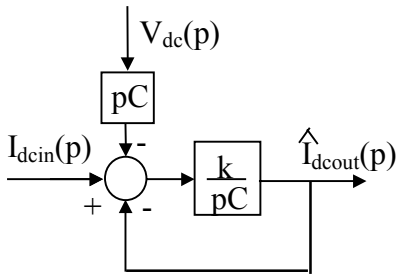

Fig. 4 The redrawn estimator.

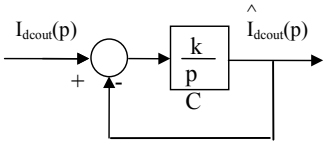

Fig. 5 The simplified block diagram.

or in another form

$$(7)\ I_{dcin}(p) - pCV_{dc}(p) = I_{dcout}(p)$$

This means that the block diagram from Fig.4 can be redrawing as in Fig. 5 (Rosu, and Gaiceanu, 1998).
The problem consists of the calculation of the parameter *k* such that the error between the estimated DC load current $\hat{I}_{dcout}(p)$ and the actual dc load current $I_{dcout}(p)$ to be insignificant. The closed loop function of the estimator, (Fig.6), derived from Fig.5, is given by:

$$(8)\ G(p) = \frac{\hat{I}_{dcout}(p)}{I_{dcout}(p)} = \frac{1}{pT_E + 1}$$

Considering a step variation for the $I_{dcout}(p)$, by setting:

$$(9)\ I_{dcout}(p) = \frac{I_{dcout}}{p}$$

the estimated dc load current get the form

$$(10)\ \hat{I}_{dcout}(p) = I_{dcout}\frac{1}{p(pT_E + 1)}$$

where

$$(11)\ T_E = \frac{C}{k}$$

is the time constant of the estimator. By adequate choosing of the *k* parameter, respectively time constant T_E (Nichita, *et al.*, 1996; Rosu and Gaiceanu, 1998), an acceptable step response $\hat{I}_{dcout}(p)$ is obtained.

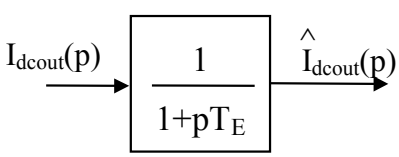

Fig. 6 The final form of the estimator.

Using Z-transform and zero order hold, the estimated dc load current can be calculated via

$$\hat{I}_{dcout}(k+1) = \hat{I}_{dcout}(k) + k\left[\frac{T_s}{C}\left(I_{dcin}(k) - \hat{I}_{dcout}(k)\right) - V_{dc}(k)\right] \quad (12)$$

where k and $k+1$ are the values of the I_{dcout}, I_{dcin}, V_{dc} at the time kT_s and $(k+1)T_s$, T_s being the sampling period.

An advantage of the estimated method is that there is no ripple presence in the feed-forward reference current of the source side. The small reference current ripple is delivered from the output of the dc link voltage controller.

5. EXPERIMENTAL RESULTS

To show the effectiveness of the proposed dc load power estimator the experimental transient performances of the system are presented for both step up (Fig.8) and sudden step down in load power (Fig.9). The 1st order power estimator was simulated and implemented using (12),(4) eqs, for an ac-ac drive system with *37kW, 1485rpm* induction motor. The overall control of the ac-ac system is implemented using two control boards (based on the dSMC 101 DSP)(Sican, 1999). Through the simulation (Fig. 10) and the experimental (Fig.11) tests, the real and the estimated dc link currents are obtained. In Fig. 12 the experimental results of the dc link voltage are presented. The dc link voltage was obtained using a test generator under a load variation between $[0.5,1]\times I_N$ (Fig. 7).

6. CONCLUSIONS

The first order dc load power estimator is presented. The experimental results confirm the realizing of a good estimation of the load power, without additional equipment. The implementation of the power estimator needs, for a complex drive control, only the completion of the software with (12),(4) eqs. The utility of the estimator is important for the torque control or for the advanced control synthesis (Leonhard, 1996).

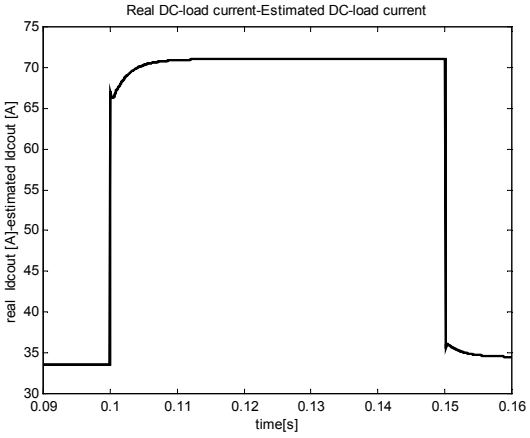

Fig. 7 Simulation results. Ch A: The real dc load current I_{dcout}, Ch B: The estimated dc link current $\hat{I}_{dcout}$.

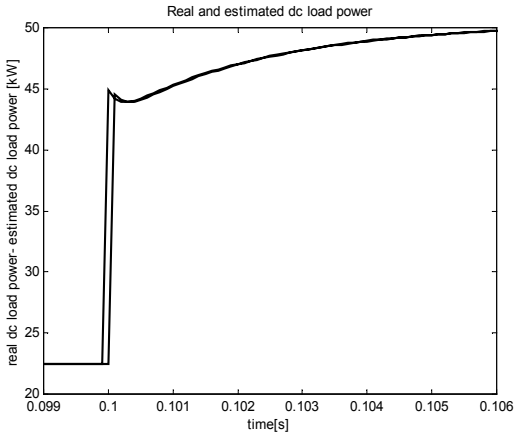

Fig. 8 Step-up. Simulation results- Ch A: The real load power P_{dc}, Ch B: The estimated load power $\hat{P}_{dc}$.

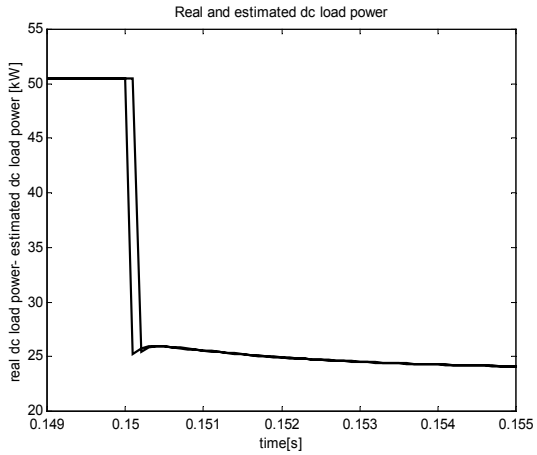

Fig. 9 Step-down. Simulation results- Ch A: The real load power P_{dc}, Ch B: The estimated load power $\hat{P}_{dc}$.

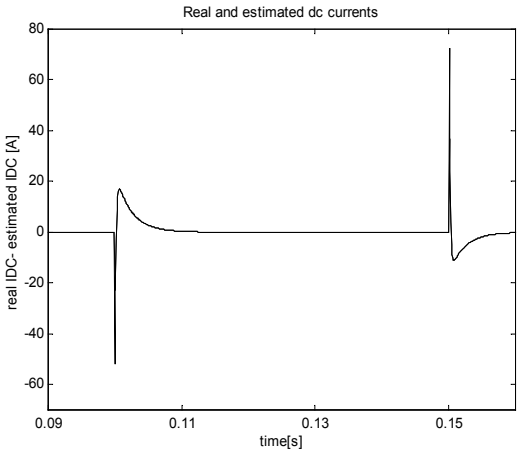

Fig. 10 Simulation results- Ch A: The real dc link load current I_{dcout}, Ch B: The estimated dc link load current $\hat{I}_{dc}$.

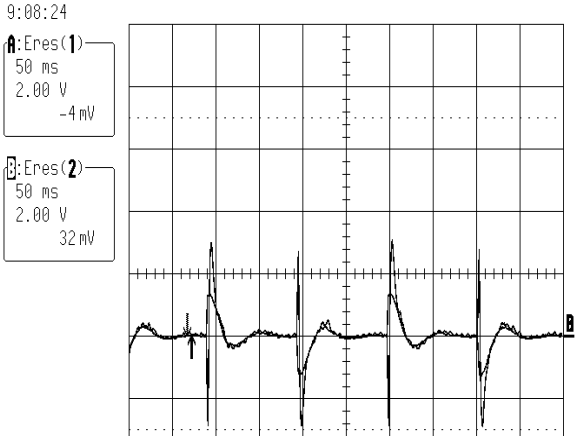

Fig. 11 Experimental results. Ch A: The real dc link current I_{dc}, Ch B: The estimated dc link current $\hat{I}_{dc}$ 30 A/div.

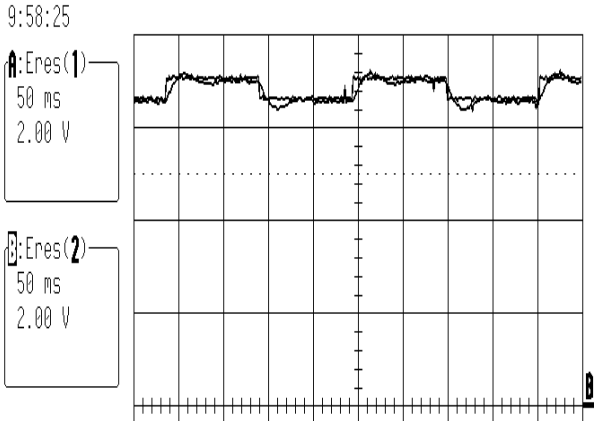

Fig. 12 Experimental results. Ch A: The DC link voltage reference. Ch.B: Actual DC link voltage. 200V/div (GenHiref=23000cnt).

The dc voltage regulation with good dynamic response is achieved even if dc capacitance is substantially reduced. This implies also the good accuracy of the dc load power estimation.

By using the estimated method, the diminished ripple in the actual current of the source side is obtained. Hence, small power losses in power components, lower current rating of power components and easier protection of the system.

For the ac-ac converter system with two control boards the method presented has an important advantage by eliminating the serial communication between them.

Another advantages of the estimated method are: no time delay, the feed-forward current component has no ripple, and more fast control response.

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